TPS2291xx, 5.5-V, 2-A, 37mΩ On-Resistance Load Switch

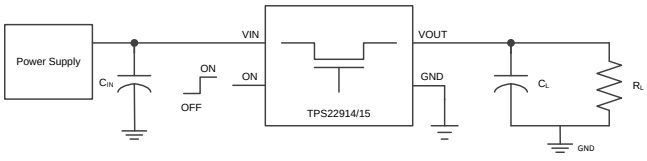
1 Features

- Integrated Single Channel Load Switch
- Input Voltage Range: 1.05 V to 5.5 V
- Low On-Resistance (R_{ON})
  - R_{ON} = 37 mΩ (typ) at V_{IN} = 5 V
  - R_{ON} = 38 mΩ (typ) at V_{IN} = 3.3 V
  - R_{ON} = 43 mΩ (typ) at V_{IN} = 1.8 V
- 2-A Maximum Continuous Switch Current
- Low Quiescent Current
  - 7.7 µA (typ) at V_{IN} = 3.3 V
- Low Control Input Threshold Enables Use of 1.0-V or Higher GPIO
- Controlled Slew Rate
  - t_R = 64 µs at V_{IN} = 3.3 V
- Quick Output Discharge (TPS22915 only)
- Ultra-Small Wafer-Chip-Scale Package
  - 0.78 mm × 0.78 mm, 0.4-mm Pitch, 0.5-mm Height (YFP)
- ESD Performance Tested per JESD 22
  - 2 kV HBM and 1 kV CDM

2 Applications

- Smartphones / Mobile Phones
- Ultrathin / Ultrabook™ / Notebook PC
- Tablet PC / Phablet
- Wearable Technology
- Solid State Drives
- Digital Cameras

4 Simplified Schematic



3 Description

The TPS22914B/15B is a small, low R_{ON}, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.05 V to 5.5 V and can support a maximum continuous current of 2 A. The switch is controlled by an on/off input, which is capable of interfacing directly with low-voltage control signals.

The small size and low R_{ON} makes the device ideal for being used in space constrained, battery powered applications. The wide input voltage range of the switch makes it a versatile solution for many different voltage rails. The controlled rise time of the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The TPS22915 further reduces the total solution size by integrating a 143-Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off.

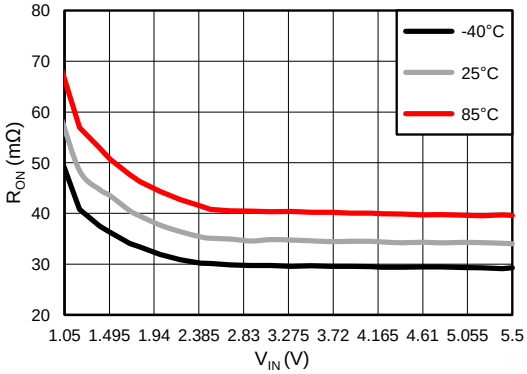
The TPS22914B/15B is available in a small, space-saving 0.78 mm x 0.78 mm, 0.4-mm pitch, 0.5-mm height 4-pin Wafer-Chip-Scale (WCSP) package (YFP). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22915B	DSBGA (4)	0.78 mm x 0.78 mm
TPS22914B		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

R_{ON} vs V_{IN} (I_{OUT} = –200 mA)



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5 Revision History

Changes from Original (June 2014) to Revision A **Page**

- Initial release of full version. ... 1

6 Device Comparison Table

DEVICE	R_{ON} at 3.3V (TYP)	t_R at 3.3V (TYP)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22914B	38 mΩ	64 µs	No	2 A	Active High
TPS22915B	38 mΩ	64 µs	Yes	2 A	Active High

7 Pin Configuration and Functions

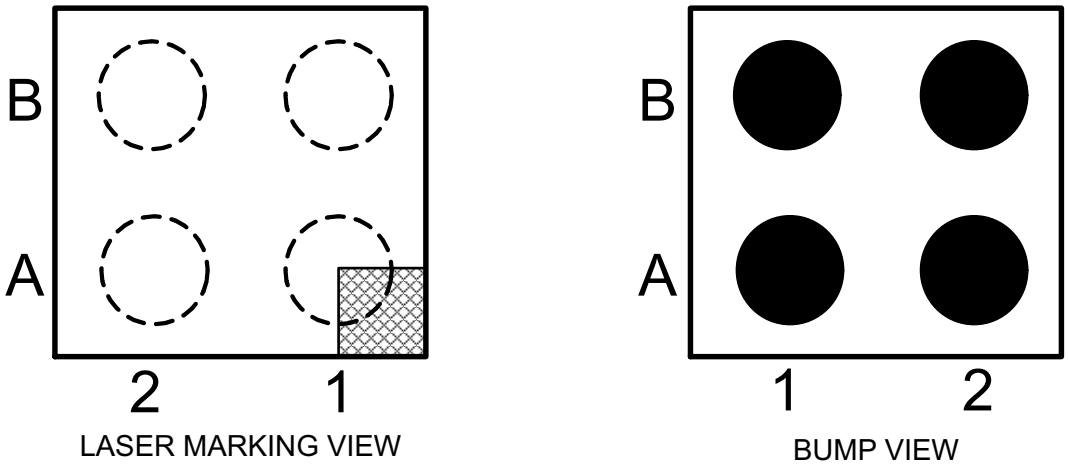


Table 1. Pin Description

B	ON	GND
A	VIN	VOUT
	2	**1**

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Switch output. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information.
VIN	A2	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information.
GND	B1	-	Device ground.
ON	B2	I	Active high switch control input. Do not leave floating.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	6	V
V_{ON}	ON voltage range	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		2.5	A
T_J	Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)			300	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2	KV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.05	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{IN} = 1.05 V to 5.5 V	1	5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{IN} = 1.05 V to 5.5 V	0	0.5	V
T_A	Operating free-air temperature range(1)		–40	85	°C
C_{IN}	Input Capacitor		1(2)		µF

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(MAX)}$], the maximum power dissipation of the device in the application [$P_{D(MAX)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(MAX)} = T_{J(MAX)} – (\theta_{JA} \times P_{D(MAX)})$.
(2) Refer to *Detailed Description* section

8.4 Thermal Information

THERMAL METRIC(1)		TPS22914 / TPS22915 YFP 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	36	
ψ_{JT}	Junction-to-top characterization parameter	12	
ψ_{JB}	Junction-to-board characterization parameter	36	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (Full). Typical values are for T_A = 25°C.

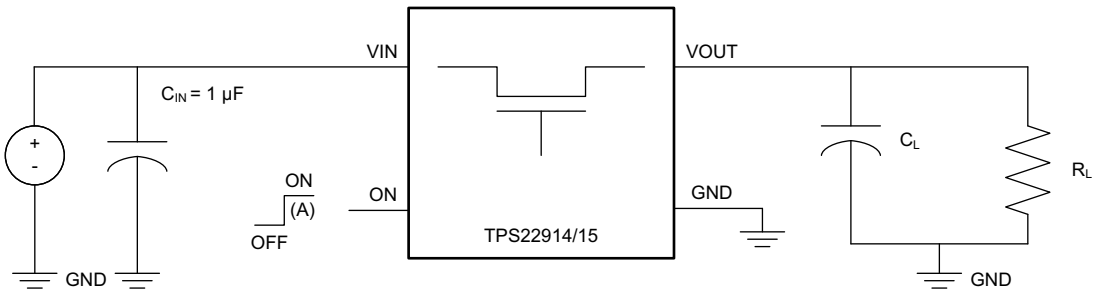
PARAMETER		TEST CONDITION		T_A	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$	Quiescent current	V_{ON} = 5 V, I_{OUT} = 0 A	V_{IN} = 5.5 V	Full		7.7	10.8	µA
			V_{IN} = 5.0 V			7.6	9.6	
			V_{IN} = 3.3 V			7.7	9.6	
			V_{IN} = 1.8 V			8.4	11.0	
			V_{IN} = 1.2 V			7.4	10.4	
			V_{IN} = 1.05 V			6.7	10.9	
$I_{SD, VIN}$	Shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 5.5 V	Full		0.5	2	µA
			V_{IN} = 5.0 V			0.5	2	
			V_{IN} = 3.3 V			0.5	2	
			V_{IN} = 1.8 V			0.5	2	
			V_{IN} = 1.2 V			0.4	2	
			V_{IN} = 1.05 V			0.4	2	
I_{ON}	ON pin input leakage current	V_{IN} = 5.5 V, I_{OUT} = 0 A		Full			0.1	µA
R_{ON}	On-Resistance	V_{IN} = 5.5 V, I_{OUT} = –200 mA		25°C		37	40	mΩ
				Full			51	
		V_{IN} = 5.0 V, I_{OUT} = –200 mA		25°C		37	41	mΩ
				Full			51	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA		25°C		37	41	mΩ
				Full			52	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA		25°C		38	41	mΩ
				Full			52	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA		25°C		38	42	mΩ
				Full			53	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA		25°C		43	48	mΩ
				Full			59	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA		25°C		52	61	mΩ
				Full			73	
		V_{IN} = 1.05 V, I_{OUT} = –200 mA		25°C		63	96	mΩ
				Full			102	
V_{HYS}	ON pin hysteresis	V_{IN} = 5.5 V		Full		102		mV
		V_{IN} = 5.0 V		Full		100		
		V_{IN} = 3.3 V		Full		98		mV
		V_{IN} = 2.5 V		Full		96		mV
		V_{IN} = 1.8 V		Full		96		
		V_{IN} = 1.2 V		Full		94		mV
		V_{IN} = 1.05 V		Full		92		
R_{PD} (1)	Output pull down resistor	V_{IN} = V_{OUT} = 3.3 V, V_{ON} = 0 V		Full		143	200	Ω

(1) TPS22915B only.

8.6 Switching Characteristics

Refer to the timing test circuit in Figure 1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the ON pin is asserted high.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		104		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		89		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		59		µs
V_{IN} = 3.3 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		83		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		64		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		52		µs
V_{IN} = 1.05 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		61		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		3		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		28		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		47		µs



A. Rise and fall times of the control signal is 100ns

Figure 1. Test Circuit

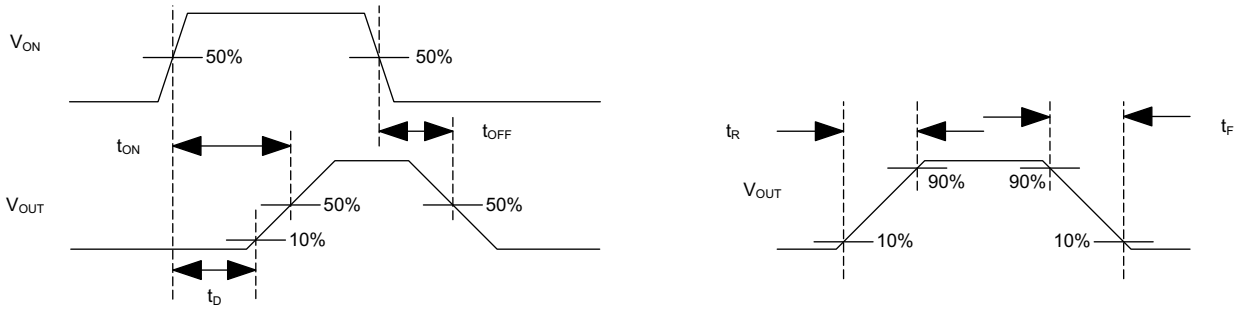
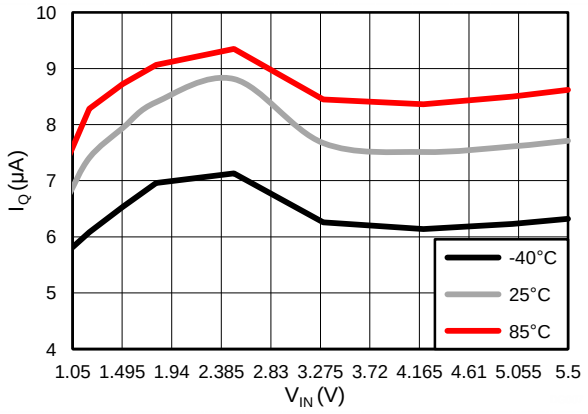


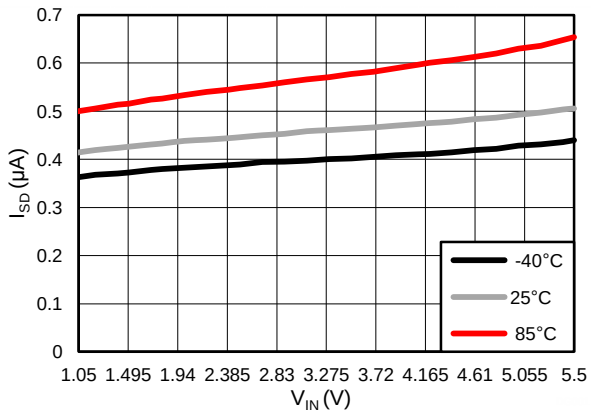
Figure 2. Timing Waveforms

8.7 Typical DC Characteristics



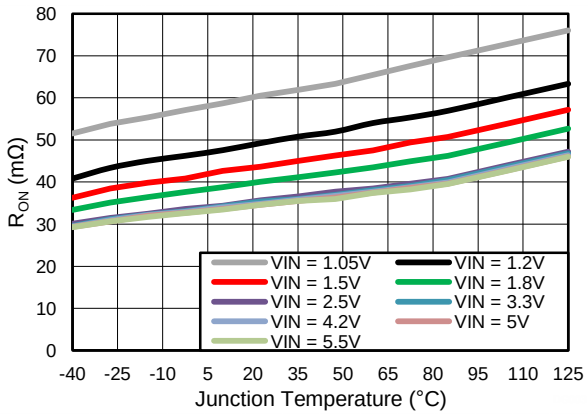
V_{ON} = 5 V I_{OUT} = 0 A

Figure 3. I_Q vs V_{IN}



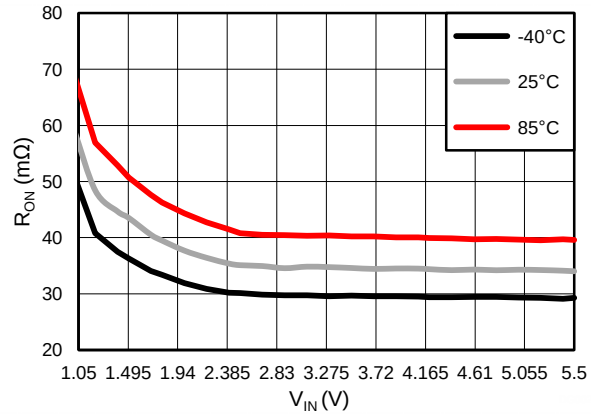
V_{ON} = 0 V I_{OUT} = 0 A

Figure 4. I_{SD} vs V_{IN}



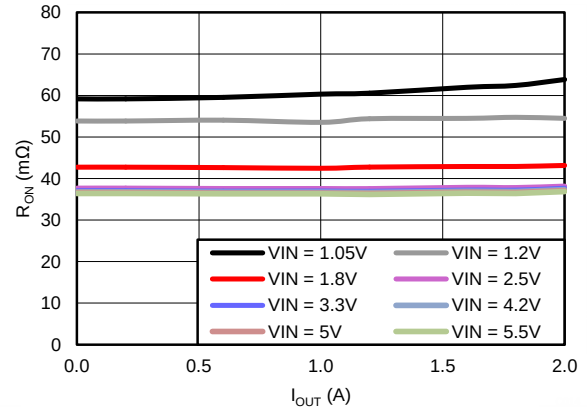
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 5. R_{ON} vs T_J



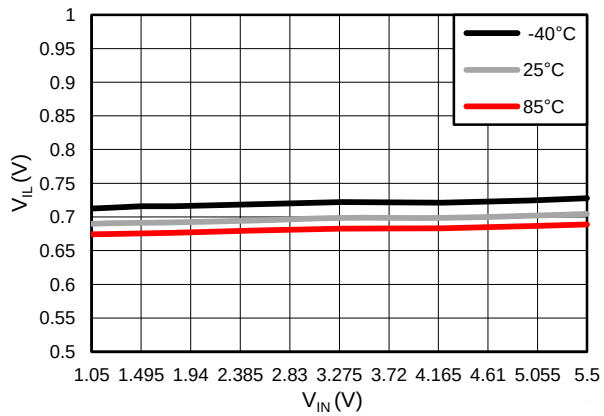
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 6. R_{ON} vs V_{IN}



V_{ON} = 5 V T_A = 25°C

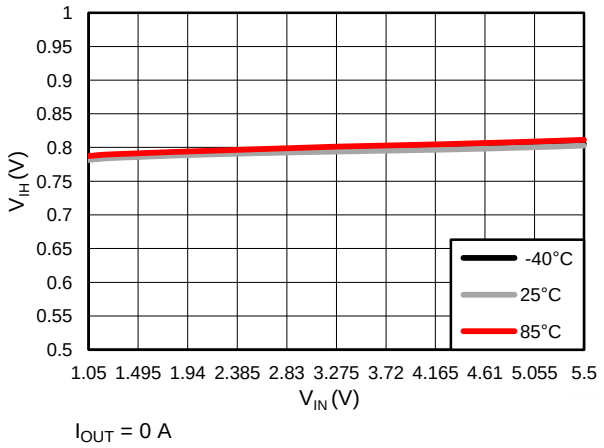
Figure 7. R_{ON} vs I_{OUT}



I_{OUT} = 0 A

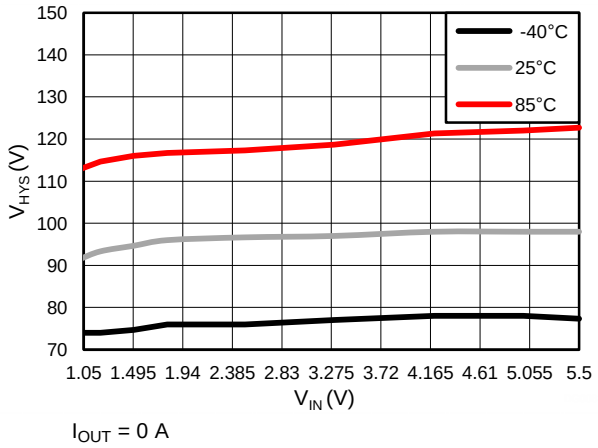
Figure 8. V_{IL} vs V_{IN}

Typical DC Characteristics (continued)



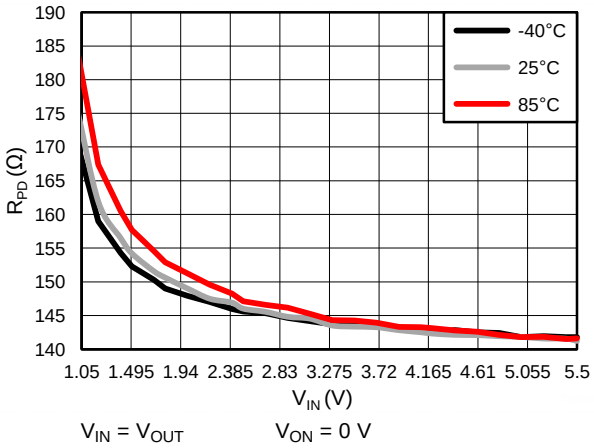
I_{OUT} = 0 A

Figure 9. V_{IH} vs V_{IN}



I_{OUT} = 0 A

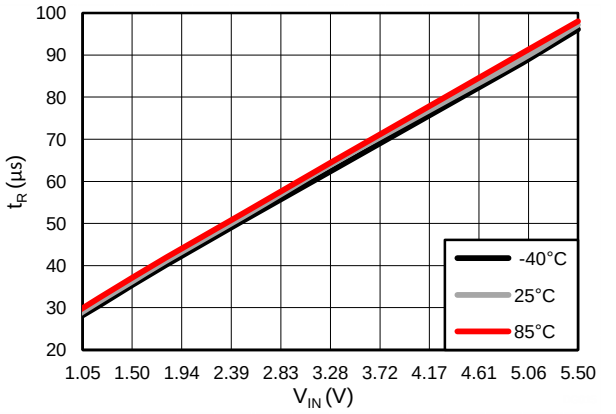
Figure 10. V_{HYS} vs V_{IN}



$V_{IN} = V_{OUT}$ V_{ON} = 0 V

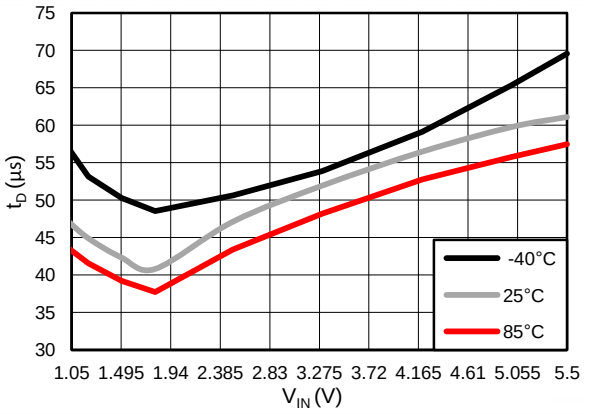
Figure 11. R_{PD} vs V_{IN}

8.8 Typical AC Characteristics



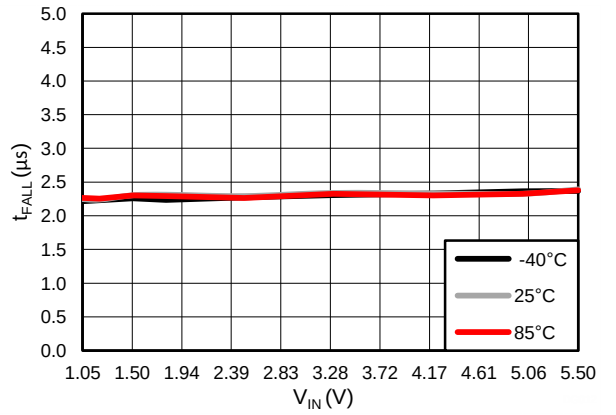
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 12. t_R vs V_{IN}



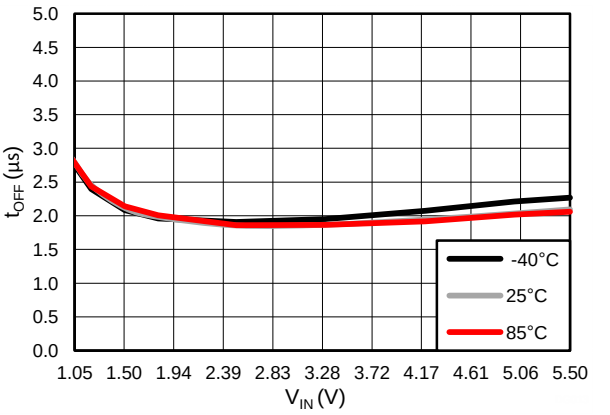
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 13. t_D vs V_{IN}



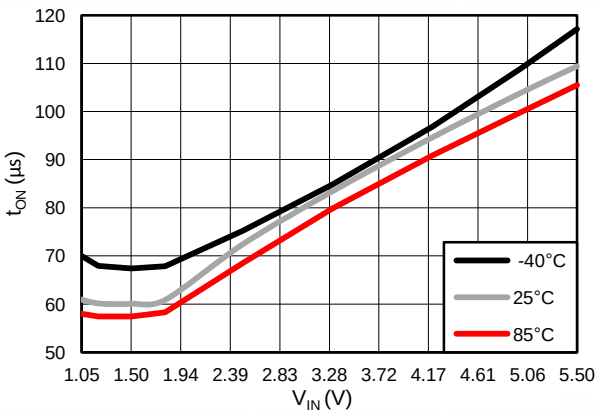
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 14. t_F vs V_{IN}



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 15. t_{OFF} vs V_{IN}



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 16. t_{ON} vs V_{IN}

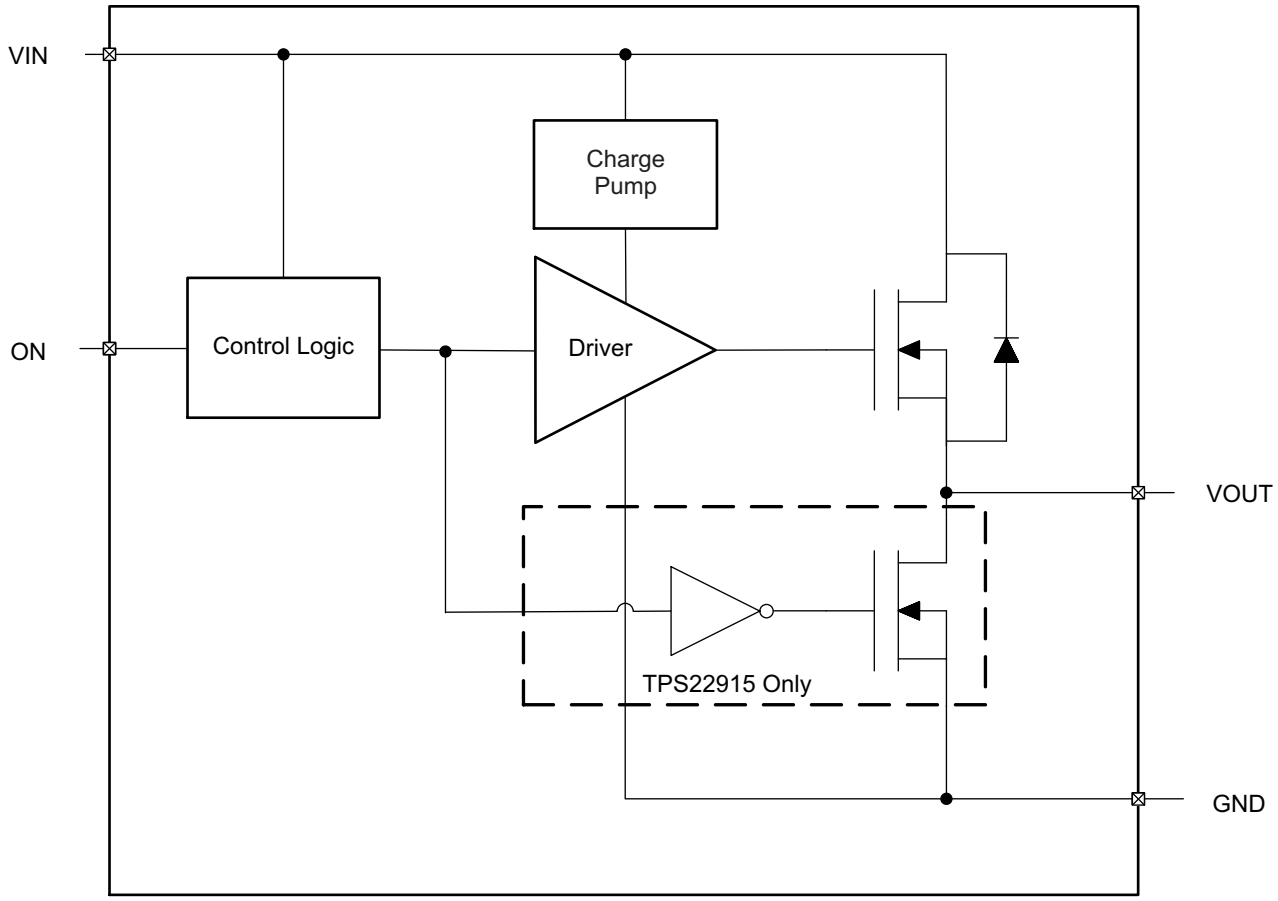
9 Detailed Description

9.1 Overview

The device is a 5.5-V, 2-A load switch in a 4-pin YFP package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On/Off Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.0-V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

Feature Description (continued)

9.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.4 Device Functional Modes

Table 2 describes the connection of the VOUT pin depending on the state of the ON pin.

Table 2. VOUT Connection

ON	TPS22914	TPS22915
L	Open	GND
H	VIN	VIN

10 Application and Implementation

10.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

10.2 Typical Application

This typical application demonstrates how the TPS22914 and TPS22915 can be used to power downstream modules.

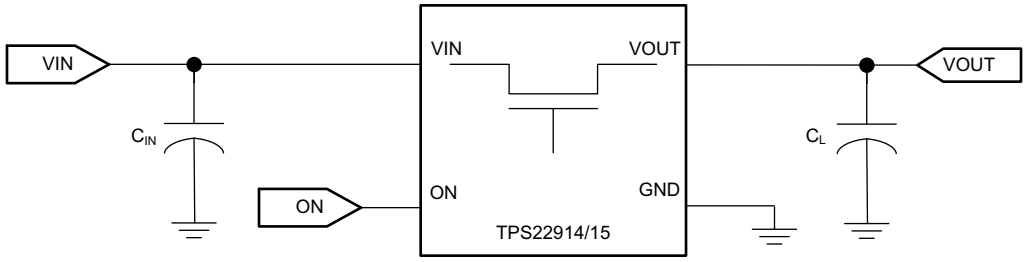


Figure 17. Typical Application Schematic

10.2.1 Design Requirements

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5.0 V
Load Current	2 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- Load Current

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

Where:

ΔV = voltage drop from VIN to VOUT
I_{LOAD} = load current
R_{ON} = On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (2)$$

Where:

I_{INRUSH} = amount of inrush caused by C_L
C_L = capacitance on VOUT
dt = rise time in VOUT during the ramp up of VOUT when the device is enabled
dV_{OUT} = change in VOUT during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

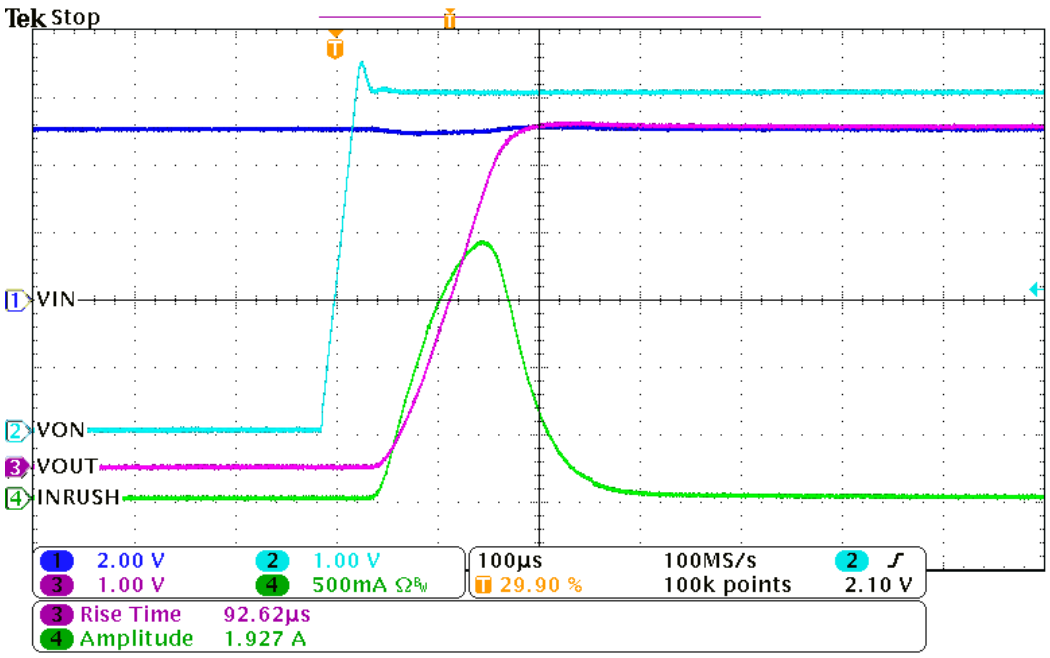
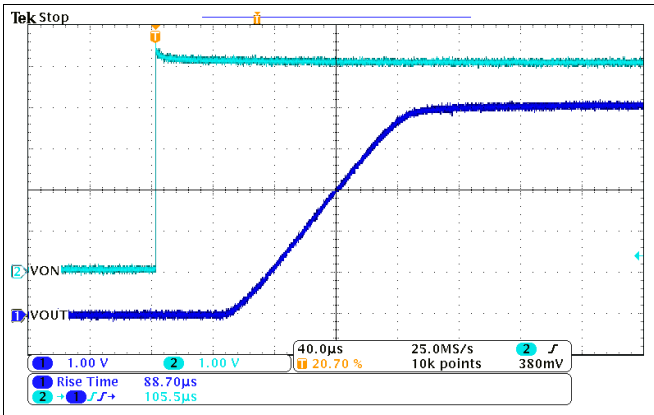


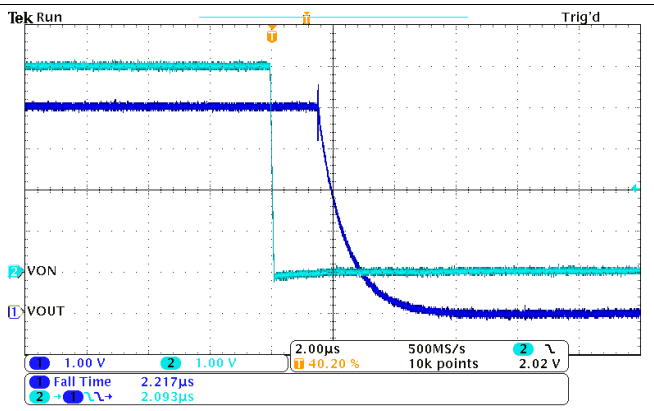
Figure 18. Inrush Current (V_{IN} = 5 V, C_L = 47 µF)

10.2.3 Application Curves



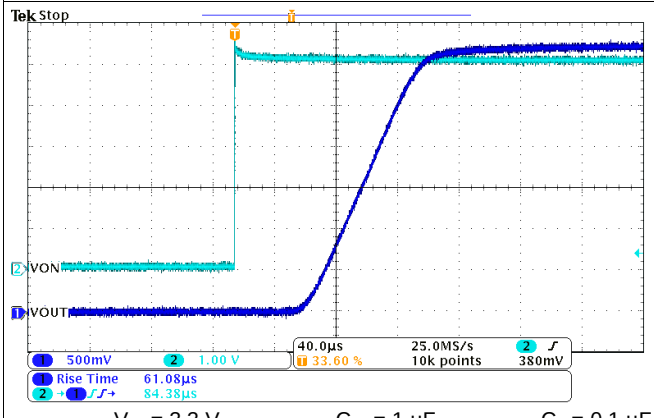
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 19. t_R at V_{IN} = 5 V



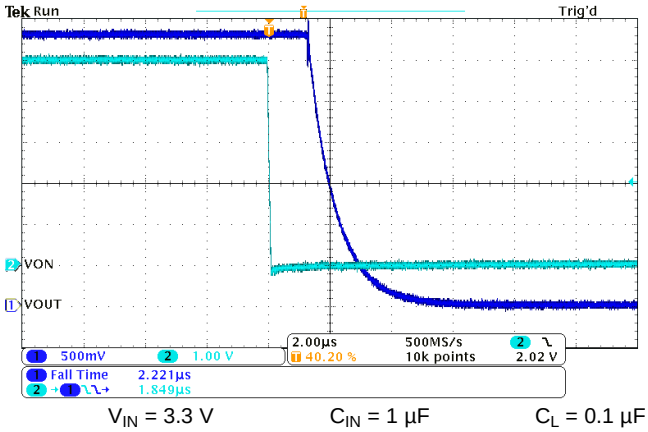
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 20. t_F at V_{IN} = 5 V



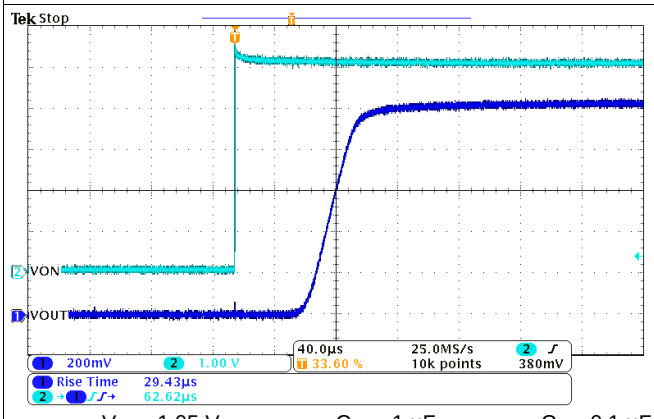
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 21. t_R at V_{IN} = 3.3 V



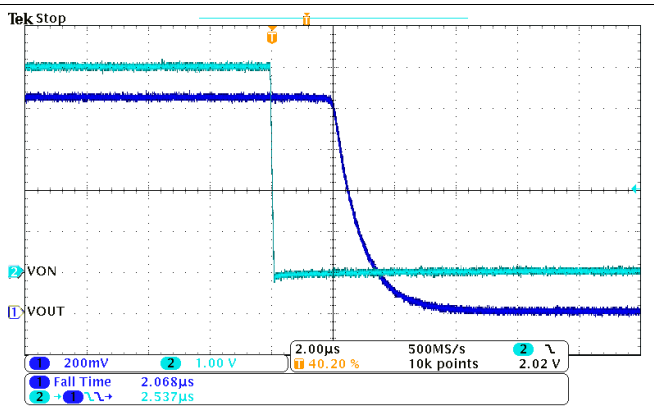
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 22. t_F at V_{IN} = 3.3V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 23. t_R at V_{IN} = 1.05V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 24. t_F at V_{IN} = 1.05 V

11 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.05 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

1. VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
2. The VIN pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
3. The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

12.1.1 Thermal Considerations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 3:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (3)$$

Where:

$P_{D(MAX)}$ = maximum allowable power dissipation
$T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22914/15)
T_A = ambient temperature of the device
θ_{JA} = junction to air thermal impedance. Refer to the *Thermal Information* table. This parameter is highly dependent upon board layout.

12.2 Layout Example

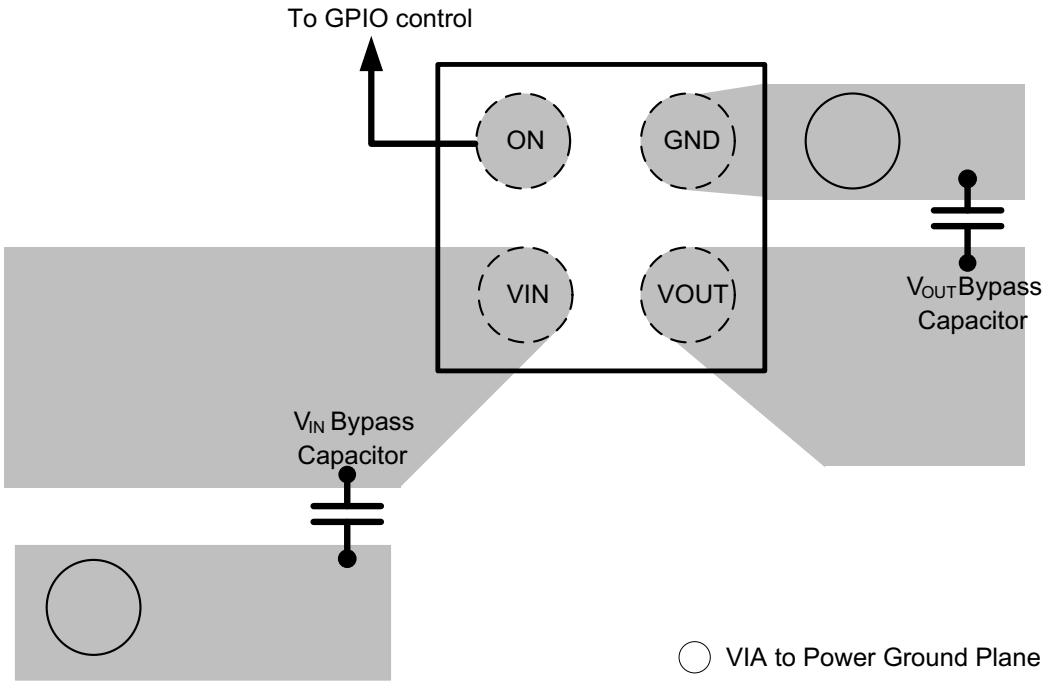


Figure 25. Recommended Board Layout

13 Device and Documentation Support

13.1 Trademarks

Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22914BYFPR	PREVIEW	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S3	
TPS22914BYFPT	PREVIEW	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S3	
TPS22915BYFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S4	Samples
TPS22915BYFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

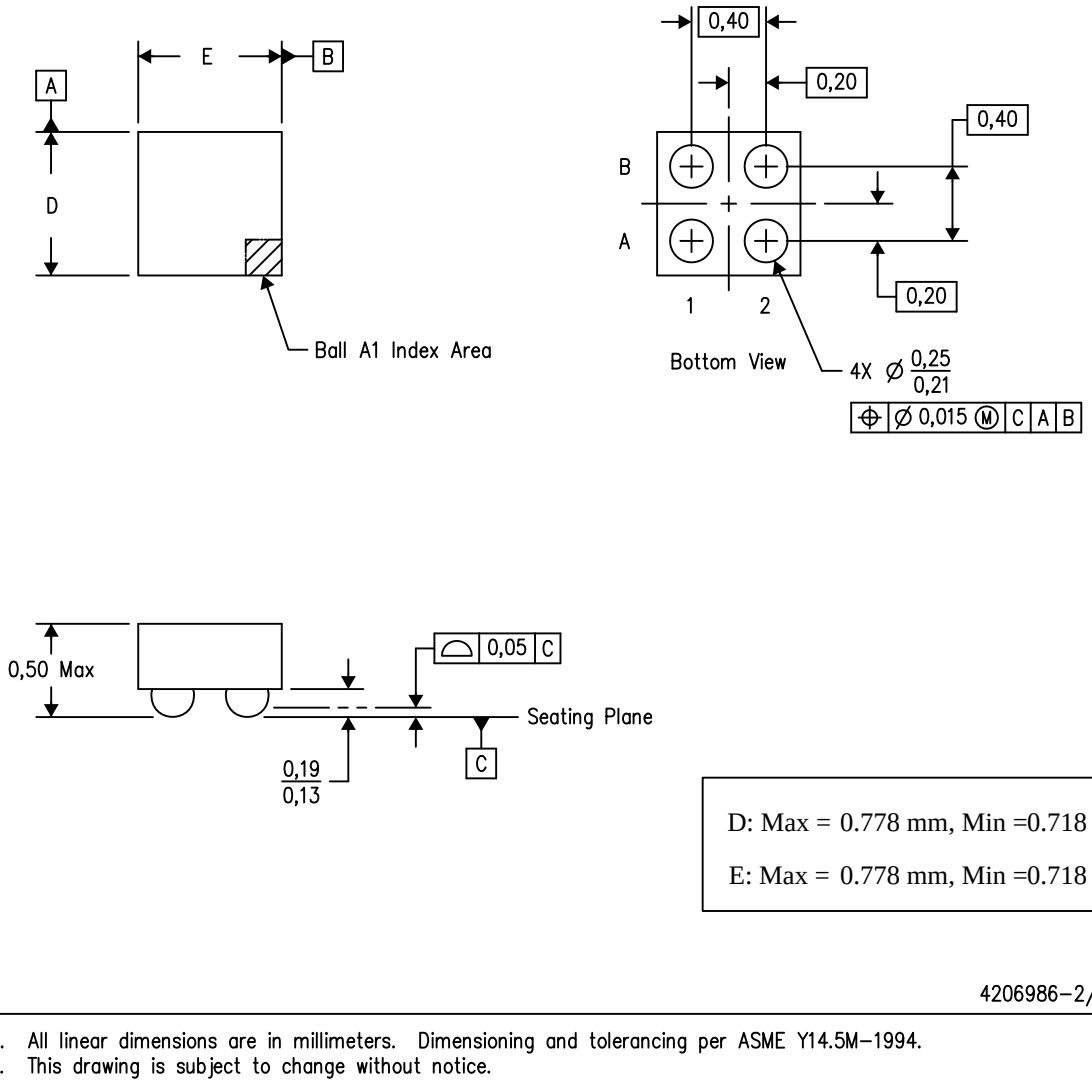
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

YFP (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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